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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,811	07/31/2003	Kouichi Nagano	60188-599	9792

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EXAMINER

BENGHUZZI, MOHSIN M

ART UNIT	PAPER NUMBER
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2611

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/630,811

Applicant(s)

NAGANO, KOUICHI

Examiner

Mohsin (Ben) Benghuzzi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on July 31, 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date July 31, 2003, July 14, 2005, Feb. 13, 2006
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (US 5,940,451).

1) Regarding claim 1:

Kim discloses a digital AGC circuit used for an address information demodulation circuit for demodulating address information recorded on a DVD by phase modulation of a wobble signal, the digital AGC circuit comprising:

a peak detection circuit for receiving a digitized wobble signal and detecting a peak value in a time period equal to or more than a half period of the wobble signal (Column 3 Lines 38-41, wherein, the magnitude estimator is interpreted as the peak detection circuit);

a gain computation circuit for computing a gain adjustment coefficient from the detected peak value (Column 4 Lines 37-40); and

a multiplier for multiplying the digitized wobble signal by the gain adjustment coefficient (Column 5 Lines 15-17).

2) Regarding claim 11:

Kim discloses a digital AGC circuit used for an address information demodulation circuit for demodulating address information recorded on a DVD by phase modulation of a wobble signal, the digital AGC circuit comprising:

a peak detection circuit for receiving an output of the digital AGC circuit and detecting a peak value in a time period equal to or more than a half period of the input (Column 3 Lines 38-41, wherein, the magnitude estimator is interpreted as the peak detection circuit);

a gain computation circuit for computing a gain adjustment coefficient from the detected peak value (Column 4 Lines 37-40); and

a multiplier for receiving a digitized wobble signal and multiplying the wobble signal by the gain adjustment coefficient (Column 5 Lines 15-17).

3. Claims 1, 2, 3, 9, 11, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Borazjani (US 5,719,867).

1) Regarding claim 1:

Borazjani discloses a digital AGC circuit used for an address information demodulation circuit for demodulating address information recorded on a DVD by phase modulation of a wobble signal, the digital AGC circuit comprising:

a peak detection circuit for receiving a digitized wobble signal and detecting a peak value in a time period equal to or more than a half period of the wobble signal (Column 22 Line 3, wherein, the amplitude detector is interpreted as the peak detection circuit, and Column 24 Lines 46-47);

a gain computation circuit for computing a gain adjustment coefficient from the detected peak value (Column 24 Lines 36-77 and Lines 40-44, wherein, the multiplying factor M is interpreted as the adjustment coefficient); and

a multiplier for multiplying the digitized wobble signal by the gain adjustment coefficient (Column 22 Lines 3-5).

2) Regarding claim 2:

Borazjani discloses the digital AGC circuit of claim 1, further comprising a delay circuit for delaying the wobble signal and supplying the delayed signal to the multiplier (Column 6 Lines 15-17).

3) Regarding claim 3:

Borazjani discloses the digital AGC circuit of claim 1, further comprising a limiter for limiting the gain adjustment coefficient to be supplied from the gain computation circuit to the multiplier to within a fixed range (Column 24 Lines 44-45, wherein, shifter limits output to the range of 0.5 to 2 times its nominal input).

4) Regarding claim 9:

Borazjani discloses the digital AGC circuit of claim 1, wherein the gain computation circuit includes a divider for dividing a reference value by the peak value detected by the peak detection circuit (Column 26 Lines 6-8 and 627 in Fig. 12, wherein, in determining the average, a divider is utilized).

5) Regarding claim 11:

Borazjani discloses a digital AGC circuit used for an address information demodulation circuit for demodulating address information recorded on a DVD by phase modulation of a wobble signal, the digital AGC circuit comprising:

a peak detection circuit for receiving an output of the digital AGC circuit and detecting a peak value in a time period equal to or more than a half period of the input (Column 22 Line 3, wherein, the amplitude detector is interpreted as the peak detection circuit, and Column 24 Lines 46-47);

a gain computation circuit for computing a gain adjustment coefficient from the detected peak value (Column 24 Lines 36-77 and Lines 40-44, wherein, the multiplying factor M is interpreted as the adjustment coefficient); and

a multiplier for receiving a digitized wobble signal and multiplying the wobble signal by the gain adjustment coefficient (Column 22 Lines 3-5).

6) Regarding claim 18:

Borazjani discloses the digital AGC circuit of claim 11, wherein the gain computation circuit includes a divider for dividing a reference value by the peak value detected by the peak detection circuit (Column 26 Lines 6-8 and 627 in Fig. 12, wherein, in determining the average, a divider is utilized).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 4-8, and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borazjani (US 5,719,867) in view of Kiyanagi et al. (US 6,029,056).

1) Regarding claim 4:

Borazjani discloses the digital AGC circuit of claim 1, wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter and supplying the detected maximum value to the gain computation circuit (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value).

Borazjani does not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

It is advantageous to use a counter in the AGC of Borazjani. Channel clock cycles must be counted in order to determine elapsed time, and therefore, determine the needed wobble signal period. Using a counter will allow for the counting of clock cycles. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

2) Regarding claim 5:

Borazjani discloses the digital AGC circuit of claim 1, wherein the peak detection circuit comprises:

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

an absolute value circuit for computing the absolute value of the detected negative peak value and supplying the computed absolute value to the gain computation circuit (Column 25 Lines 51-54).

Borazjani does not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

3) Regarding claim 6:

Borazjani discloses the digital AGC circuit of claim 1, wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period

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counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to the output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

a selector for selecting either the detected positive peak value or negative peak value and supplying the selected peak value to the gain computation circuit (Column 28 Lines 14-17).

Borazjani does not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

4) Regarding claim 7:

Borazjani discloses the digital AGC circuit of claim 1, wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period

counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to the output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

a difference circuit for computing the difference between the detected positive peak value and negative peak value and supplying the computed difference to the gain computation circuit (Column 25 Lines 54-56, wherein, subtracting is interpreted as computing the difference).

Borazjani does not disclose, a one-period counter for counting one period of the wobble signal. However, as discussed above in claim 4, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

5) Regarding claim 8:

Borazjani discloses the digital AGC circuit of claim 1, wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in a half period of the wobble signal as a positive peak value according to an output of the half-period

counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in a half period of the wobble signal as a negative peak value according to the output of the half-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

an adder for adding the detected positive peak value and negative peak value (Column 26 Line 62-63);

a selector for selecting either the detected positive peak value or negative peak value according to an output of the adder and supplying the selected peak value to the gain computation circuit (Column 28 Lines 14-17).

Borazjani does not disclose, a half-period counter for counting a half period of the wobble signal. However, Kiyanagi et al. discloses, a half-period counter for counting a half period of the wobble signal (Column 9 Lines 13-14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a half-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal half-period.

6) Regarding claim 12:

Kiyanagi et al. further discloses, further comprising an integrator for integrating the gain adjustment coefficient received from the gain computation circuit and supplying the result to the multiplier (Column 9 Lines 12-13).

7) Regarding claim 13:

Borazjani discloses the digital AGC circuit of claim 11, wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter and supplying the detected maximum value to the gain computation circuit (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value).

Borazjani does not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

8) Regarding claim 14:

Borazjani discloses the digital AGC circuit of claim 11, wherein the peak detection circuit comprises:

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

an absolute value circuit for computing the absolute value of the detected negative peak value and supplying the computed absolute value to the gain computation circuit (Column 25 Lines 51-54).

Borazjani does not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

9) Regarding claim 15:

Borazjani discloses the digital AGC circuit of claim 11, wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

a selector for selecting either the detected positive peak value or negative peak value and supplying the selected peak value to the gain computation circuit (Column 28 Lines 14-17).

Borazjani does not disclose, a one-period counter for counting one period of the wobble signal. However, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14).

Therefore, as discussed in claim 4 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

10)Regarding claim 16:

Borazjani discloses the digital AGC circuit of claim 11, wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

a difference circuit for computing the difference between the detected positive peak value and negative peak value and supplying the computed difference to the gain computation circuit (Column 25 Lines 54-56, wherein, subtracting is interpreted as computing the difference).

Borazjani does not disclose, a one-period counter for counting one period of the wobble signal. However, as discussed above in claim 4, Kiyanagi et al. discloses, a one-period counter for counting one period of the wobble signal (Column 9 Lines 13-14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a one-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal period.

11)Regarding claim 17:

Borazjani discloses the digital AGC circuit of claim 11, wherein the peak detection circuit comprises:

a maximum detection circuit for detecting the maximum value in a half period of the wobble signal as a positive peak value according to an output of the half-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the maximum value);

a minimum detection circuit for detecting the minimum value in a half period of the wobble signal as a negative peak value according to an output of the half-period counter (Column 22 Line 3, wherein, the amplitude detector is inherently capable of detecting the minimum value);

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an adder for adding the detected positive peak value and negative peak value (Column 26 Line 62-63);

a selector for selecting either the detected positive peak value or negative peak value according to an output of the adder and supplying the selected peak value to the gain computation circuit (Column 28 Lines 14-17).

Borazjani does not disclose, a half-period counter for counting a half period of the wobble signal. However, Kiyanagi et al. discloses, a half-period counter for counting a half period of the wobble signal (Column 9 Lines 13-14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a half-period counter, as Kiyanagi et al. teaches, in the AGC circuit of Borazjani in order to be able to count clock cycles, and therefore, be able to determine wobble signal half-period.

6. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borazjani (US 5,719,867) in view of Tenca et al. (US 7,046,800).

1) Regarding claim 10:

Borazjani discloses the digital AGC circuit of claim 9 but does not disclose, wherein the divider is constructed of a bit shift circuit for performing bit shift division. However, Tenca et al. discloses, wherein the divider is constructed of a bit shift circuit for performing bit shift division (Column 2 Lines 18-20).

It is advantageous to employ bit-shift division. Bit-shift division is a simple operation and is easy to implement (See Tenca et al., Column 2 Lines 18-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to use bit-shift division, as Tenca et al teaches, in the AGC of Borazjani in order to simplify the division operation.

2) Regarding claim 19:

Borazjani discloses the digital AGC circuit of claim 18 but does not disclose, wherein the divider is constructed of a bit shift circuit for performing bit shift division. However, Tenca et al. discloses, wherein the divider is constructed of a bit shift circuit for performing bit shift division (Column 2 Lines 18-20).

Therefore, as discussed in claim 10 above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use bit-shift division, as Tenca et al teaches, in the AGC of Borazjani in order to simplify the division operation.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Haefner et al. (US 5,620,466) discloses a digital automatic gain control using separate gain control and threshold templating.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsin (Ben) Benghuzzi whose telephone number is (571) 270-1075. The examiner can normally be reached on 8:30- 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



JAY K. PATEL
SUPERVISORY PATENT EXAMINER

Mohsin (Ben) Benghuzzi

October 4, 2006